

APPLICATION
FOR
UNITED STATES LETTERS PATENT

RECEIVED
TITLE: IMPROVED INTEGRATED CHIP PACKAGE HAVING
INTERMEDIATE SUBSTRATE

APPLICANT: SEHAT SUTARDJA

CERTIFICATE OF MAILING BY EXPRESS MAIL

Express Mail Label No. EL870690834US

I hereby certify under 37 CFR §1.10 that this correspondence is being deposited with the United States Postal Service as Express Mail Post Office to Addressee with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

September 27, 2001

Date of Deposit

Signature

Michael Hubbard

Typed or Printed Name of Person Signing Certificate

IMPROVED INTEGRATED CHIP PACKAGE HAVING INTERMEDIATE
SUBSTRATE

TECHNICAL FIELD

[0001] The present invention relates to integrated circuit packaging, and more particularly to packaging of flip chip semiconductors.

BACKGROUND

[0002] The drive to higher semiconductor device densities places increased demands on the packaging for these devices to remove heat generated from dissipated power in the device. One low cost packaging technique that has been used device having lower densities is plastic ball gate array (PBGA). In a PBGA thermal vias on the underside of the encapsulated die provide a thermal path for the thermal energy to the circuit board. Typically, a PBGA is limited to dissipating less than approximately 2.5 watts. The low power dissipation capability of a PBGA is quickly being exceeded by the power requirements of today's high density devices. In addition, routing the thermal energy into the circuit board limits the number of semiconductor devices that can be mounted on the circuit board.

[0003] Flip chip ball gate array (FCBGA) is a packaging technique that is capable of supporting semiconductor devices

that dissipate more than 20 watts of power. In a FCBGA, the semiconductor device or integrated circuit chip is connected to a package substrate via solder balls. The package substrate is coupled to the circuit board through solder balls on the underside of the package. To connect the pads of the device or chip to the solder balls, the package substrate typically uses a build-up construction to permit the use of extremely fine pitch wiring for the interconnection. Although a FCBGA provides a packaging solution for high dissipation devices, the cost of a FCBGA is very high due to the need for a substrate having a build-up construction.

SUMMARY

[0004] The present integrated chip package provides a low cost package that is suitable for high density semiconductors that have high power dissipation. The integrated chip package includes at least one semiconductor chip having a first surface and a second surface. The first surface of the semiconductor chip is electrically coupled to an intermediate substrate via conductive bumps. The intermediate substrate is also electrically coupled to a package substrate via a plurality of bonding wires. The second surface of the semiconductor chip is thermally coupled to a heat sink to increase the power dissipation capacity of the integrated chip package.

[0005] The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

[0006] Figure 1 shows a first embodiment of an integrated chip package in accordance with the principles of the invention;

[0007] Figure 2 shows a shows a second embodiment of an integrated chip package in accordance with the principles of the invention;

[0008] Figure 3A shows an interface of an intermediate substrate to a semiconductor chip;

[0009] Figure 3B shows an equivalent circuit diagram of an interface of an intermediate substrate to a semiconductor chip;

[0010] Figure 4 shows an embodiment of an intermediate substrate; and

[0011] Figure 5 shows a method of manufacturing an integrated chip package in accordance with the principles of the invention.

[0012] Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

[0013] Referring to Figure 1, a first embodiment of an integrated chip package 10 in accordance with the principles of the invention is shown. The integrated chip package 10 is a modified FCBGA that can advantageously dissipate approximately the same amount of heat as a flip chip package at a much lower cost. In addition, the thermal path of the integrated chip package 10 extends away from the circuit board to reduce the heat load on the circuit board.

[0014] The integrated chip package 10 includes a semiconductor chip 12 configured for flip chip mounting that is attached to an intermediate substrate 14. A first surface 16 of the semiconductor chip 12 is electrically connected to the intermediate substrate 14 via conductive bumps 18. The conductive bumps 18 may be formed from any electrically conductive material such as Pb/Sn solder, Au, Ag, alloys of Au and Ag, and metallic coated polymeric studs. In addition, an epoxy 13 or other suitable material formed between the conductive bumps 18 may be used as an embedding material for the conductive bumps 18 to provide mechanical support and moisture protection. The semiconductor chip 12 may be attached to the intermediate substrate 14 using any flip chip compatible bonding

method such as thermocompression, soldering, encapsulation, and adhesives.

[0015] The other surface 20 of the semiconductor chip 12 is attached to a heat sink 22 for coupling heat away from the semiconductor chip 12. The heat sink 22 may be made of any thermally conductive material such as copper and thermally conductive plastic. The semiconductor chip 12 may be attached to the heat sink 22 by any attachment item 24 that does not thermally isolate the semiconductor chip 12 such as adhesive, solder, and press-fitting by applying a mechanical force to the first surface of the semiconductor chip 12 or the intermediate substrate 14. For example, a thermally conductive epoxy may be used as the attachment item 24.

[0016] The intermediate substrate 14 is electrically connected to conductors on a package substrate 26 via several bonding wires 28. The intermediate substrate 14 converts flip chip mounting of the semiconductor chip 12 into wire bond mounting to combine and exceed the advantages of FCBGA and PBGA. Similar to FCBGA, the integrated chip package 10 provides a low resistance thermal path for heat generated in the semiconductor chip 12 so that power dissipation exceeding 20 watts may be accommodated. In addition, the thermal path of the integrated chip package 10 extends to the heat sink 22, away from the

package substrate 26, thereby reducing the heat load of the circuit board or circuit substrate to which the integrated chip package 10 is connected. Also, the integrated chip package may employ a substrate that is as inexpensive as substrates used for PBGA packages. Additionally, using the intermediate substrate 14 reduces the wiring pitch requirements on bonding wire equipment used for attaching the bonding wires 28.

[0017] Referring to Figures 1 and 2, the intermediate substrate 14 may be made from any substrate material such as normal silicon wafer (either low or high quality), polysilicon, and glass. Circuit planes such as power planes, ground planes, and interconnect planes may be added to the intermediate substrate 14. The process technology used for the circuit planes is not limited to the technology used for the semiconductor chip 12. Instead, other process technologies including lower cost technologies such as 1 micron technology may be employed to reduce the cost of the package 10. The circuit planes may provide interconnect within the semiconductor chip 12 as well as to the package substrate 26 through the bonding wires 28. Including circuit planes in the intermediate substrate 14 may reduce the requirement for expensive power and ground grids on the semiconductor chip. For example at 0.13 um, each layer of metalization costs about 10 times more than the

cost of providing the same function on the intermediate substrate 14. Moreover, the semiconductor chip 12 may employ distributed power and ground conductive bumps to achieve substantially lower impedance. Decoupling capacitors 32 may be included on the intermediate substrate to provide local filtering of power and ground signals. Providing local filtering is particularly advantageous in view of the high DC and AC currents that may flow between the intermediate substrate 18 and the semiconductor chip 12. For example, in a 20 watt device operated with 1 volt supply voltage, the DC current is 20 amps with an AC current that may be 150 amps. In view of such high magnitude AC currents, providing local filtering with low inductance paths is crucial to maintain a relatively constant supply voltage. The decoupling capacitors 32 may include one or more small capacitors as well as a single large parallel plate capacitor 31 covering the whole substrate. The values of the capacitors may be controlled by varying the thickness and area of the dielectric. For example, the value of a parallel plate capacitor 31 may be controlled by varying the thickness of a layer of silicon between the metallized plates. Additional capacitor materials may be used that otherwise are generally not used in advanced wafer fabrication because of concerns with contaminating the wafer. Examples of capacitor materials

include standard oxides and nitride oxides. In addition, trench capacitors 33 may be formed on the intermediate substrate 14. Trench capacitors advantageously provide higher volumetric efficiency than parallel plate capacitors. Practically one entire side of the intermediate substrate 14 may be used for decoupling capacitors 32, as well as portions of the other side of the intermediate substrate 14.

[0018] The package substrate 26 may be made of any substrate material suitable for ball grid array mounting to a device such as a circuit board or substrate. Additionally, a support layer 25 such as an epoxy or other suitable material may be inserted between the intermediate substrate 18 and the package 26 to provide addition mechanical support.

[0019] Shown in Figure 3A is an expanded view of the interface of the intermediate substrate 14 to the semiconductor chip 12 via the conductive bumps 18. The intermediate substrate 14 may include several metalization layers 27 separated by insulation layers 28. The conductive bumps 18 are aligned with the metalization layers 27 to provide an electrical connection between the intermediate substrate 14 and the semiconductor chip 12. The metalization layers 27 and insulation layers 28 may be configured to form local decoupling capacitors.

[0020] Shown in Figure 3B is a circuit diagram illustrating the interface shown in Figure 3A. Capacitors 29a and 29b represent the capacitance formed between the metalization layers 27.

[0021] Shown in Figure 4 is a second embodiment of an integrated chip package 40 in accordance with the principles of the invention is shown. The integrated chip package 40 is similar in function to the integrated chip package 10, with corresponding elements numbered in the range 40-60, except that the integrated chip package 40 includes several semiconductor chips 42a and 42b attached to each intermediate substrate 44 to form a multichip module (MCM). In this embodiment, semiconductor chip 42a may be a logic circuit and semiconductor chip 42b may be a power device. Any combination of semiconductor chips 42 may be used including all logic devices, all power devices, or a mix of logic devices and power devices. In addition, the quantity of semiconductor chips that may be mounted within the integrated chip package 40 is not limited to merely two. The intermediate substrate 44 may be used to provide interconnects within the semiconductor chips 42a and 42b, among the semiconductor chips 42a and 42b, and from the semiconductor chips 42a and 42b to the conductive bumps 60. Thousands of bonding wires may be provided between the

intermediate substrate 14 and the package substrate 56 for very low cost. Since many of the interconnects between the semiconductor chips 44 are made on the intermediate substrate 44, the quantity of bonding wire interconnects within the integrated chip package 40 may be significantly reduced. This is particularly advantageous with system on a package (SOP), where the power dissipation of devices within the package 40 exceeds 20 watts.

[0022] Shown in Figure 5 is a method of manufacturing an integrated chip package 10 in accordance with the principles of the invention. At block 70 a semiconductor chip to be packaged is provided. The semiconductor chip is flip chip mounted to an intermediate substrate, block 72. The semiconductor chip is then thermally attached to a heat sink, block 74. At block 76, bonding wires are connected between the intermediate substrate and a package substrate. At block 78, conductors that are suitable for ball gate array mounting are formed on the package substrate.

[0023] A number of embodiments of the invention have been described. It is expressly intended that the foregoing description and accompanying drawings are illustrative of preferred embodiments only, not limiting, and that the true spirit and scope of the present invention will be determined by

reference to the appended claims and their legal equivalent. It will be equally apparent and is contemplated that various modifications and/or changes may be made in the illustrated embodiments without departure from the spirit and scope of the invention. For example, the steps of the method of manufacturing may be performed in numerous different sequences. Accordingly, other embodiments are within the scope of the following claims.

1900 1901 1902 1903 1904 1905 1906 1907 1908 1909 1910 1911 1912 1913 1914 1915 1916 1917 1918 1919 1920 1921 1922 1923 1924 1925 1926 1927 1928 1929 1930 1931 1932 1933 1934 1935 1936 1937 1938 1939 1940 1941 1942 1943 1944 1945 1946 1947 1948 1949 1950 1951 1952 1953 1954 1955 1956 1957 1958 1959 1960 1961 1962 1963 1964 1965 1966 1967 1968 1969 1970 1971 1972 1973 1974 1975 1976 1977 1978 1979 1980 1981 1982 1983 1984 1985 1986 1987 1988 1989 1990 1991 1992 1993 1994 1995 1996 1997 1998 1999 2000 2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035 2036 2037 2038 2039 2040 2041 2042 2043 2044 2045 2046 2047 2048 2049 2050 2051 2052 2053 2054 2055 2056 2057 2058 2059 2060 2061 2062 2063 2064 2065 2066 2067 2068 2069 2070 2071 2072 2073 2074 2075 2076 2077 2078 2079 2080 2081 2082 2083 2084 2085 2086 2087 2088 2089 2090 2091 2092 2093 2094 2095 2096 2097 2098 2099 2100 2101 2102 2103 2104 2105 2106 2107 2108 2109 2110 2111 2112 2113 2114 2115 2116 2117 2118 2119 2120 2121 2122 2123 2124 2125 2126 2127 2128 2129 2130 2131 2132 2133 2134 2135 2136 2137 2138 2139 2140 2141 2142 2143 2144 2145 2146 2147 2148 2149 2150 2151 2152 2153 2154 2155 2156 2157 2158 2159 2160 2161 2162 2163 2164 2165 2166 2167 2168 2169 2170 2171 2172 2173 2174 2175 2176 2177 2178 2179 2180 2181 2182 2183 2184 2185 2186 2187 2188 2189 2190 2191 2192 2193 2194 2195 2196 2197 2198 2199 2200 2201 2202 2203 2204 2205 2206 2207 2208 2209 2210 2211 2212 2213 2214 2215 2216 2217 2218 2219 2220 2221 2222 2223 2224 2225 2226 2227 2228 2229 2230 2231 2232 2233 2234 2235 2236 2237 2238 2239 2240 2241 2242 2243 2244 2245 2246 2247 2248 2249 2250 2251 2252 2253 2254 2255 2256 2257 2258 2259 2260 2261 2262 2263 2264 2265 2266 2267 2268 2269 2270 2271 2272 2273 2274 2275 2276 2277 2278 2279 2280 2281 2282 2283 2284 2285 2286 2287 2288 2289 2290 2291 2292 2293 2294 2295 2296 2297 2298 2299 2300 2301 2302 2303 2304 2305 2306 2307 2308 2309 2310 2311 2312 2313 2314 2315 2316 2317 2318 2319 2320 2321 2322 2323 2324 2325 2326 2327 2328 2329 2330 2331 2332 2333 2334 2335 2336 2337 2338 2339 2340 2341 2342 2343 2344 2345 2346 2347 2348 2349 2350 2351 2352 2353 2354 2355 2356 2357 2358 2359 2360 2361 2362 2363 2364 2365 2366 2367 2368 2369 2370 2371 2372 2373 2374 2375 2376 2377 2378 2379 2380 2381 2382 2383 2384 2385 2386 2387 2388 2389 2390 2391 2392 2393 2394 2395 2396 2397 2398 2399 2400 2401 2402 2403 2404 2405 2406 2407 2408 2409 2410 2411 2412 2413 2414 2415 2416 2417 2418 2419 2420 2421 2422 2423 2424 2425 2426 2427 2428 2429 2430 2431 2432 2433 2434 2435 2436 2437 2438 2439 2440 2441 2442 2443 2444 2445 2446 2447 2448 2449 2450 2451 2452 2453 2454 2455 2456 2457 2458 2459 2460 2461 2462 2463 2464 2465 2466 2467 2468 2469 2470 2471 2472 2473 2474 2475 2476 2477 2478 2479 2480 2481 2482 2483 2484 2485 2486 2487 2488 2489 2490 2491 2492 2493 2494 2495 2496 2497 2498 2499 2500 2501 2502 2503 2504 2505 2506 2507 2508 2509 2510 2511 2512 2513 2514 2515 2516 2517 2518 2519 2520 2521 2522 2523 2524 2525 2526 2527 2528 2529 2530 2531 2532 2533 2534 2535 2536 2537 2538 2539 2540 2541 2542 2543 2544 2545 2546 2547 2548 2549 2550 2551 2552 2553 2554 2555 2556 2557 2558 2559 2560 2561 2562 2563 2564 2565 2566 2567 2568 2569 2570 2571 2572 2573 2574 2575 2576 2577 2578 2579 2580 2581 2582 2583 2584 2585 2586 2587 2588 2589 2590 2591 2592 2593 2594 2595 2596 2597 2598 2599 2600 2601 2602 2603 2604 2605 2606 2607 2608 2609 2610 2611 2612 2613 2614 2615 2616 2617 2618 2619 2620 2621 2622 2623 2624 2625 2626 2627 2628 2629 2630 2631 2632 2633 2634 2635 2636 2637 2638 2639 2640 2641 2642 2643 2644 2645 2646 2647 2648 2649 2650 2651 2652 2653 2654 2655 2656 2657 2658 2659 2660 2661 2662 2663 2664 2665 2666 2667 2668 2669 2670 2671 2672 2673 2674 2675 2676 2677 2678 2679 2680 2681 2682 2683 2684 2685 2686 2687 2688 2689 2690 2691 2692 2693 2694 2695 2696 2697 2698 2699 2700 2701 2702 2703 2704 2705 2706 2707 2708 2709 2710 2711 2712 2713 2714 2715 2716 2717 2